forming a third insulating film on said second insulating film, said third insulating film being made of a material different from that of the second insulating film and having a thickness larger than that of the second insulating film;

forming a groove in a region of said third insulating film, in which a wiring is to be formed, said groove having a bottom to which said second insulating film is exposed;

forming a metal wiring in said groove; and

removing a part of that portion of the second insulating film which is exposed to the groove, and a part of the first insulating film under the portion of the second insulating film, and thus forming a contact hole reaching to the semiconductor substrate, wherein the contact hole is buried with a metal in the step of forming a metal wiring in said groove.

36. (Amended) The process according to claim 29, further comprising the step of forming a barrier film on inner surfaces of said groove.

40. (Amended) A process of fabricating a semiconductor device comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a second insulating film on said first insulating film, said second insulating film being made of a material different from that of the first insulating film and having a thickness smaller than that of the first insulating film;

forming a third insulating film on said second insulating film, said third insulating film being made of a material different from that of the second insulating film and having a thickness larger than that of the second insulating film;

forming a groove in said third insulating film having a bottom comprising said second insulating film; and

forming a wiring material in said groove,

wherein said step of forming said groove comprises;

etching through said second insulation film to expose said first insulation film while leaving a remaining second portion of said second insulation film;

removing a third portion of said first insulation film to expose said substrate while leaving a remaining fourth portion of said first insulation film.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 29-40 are now present in this application, claims 28 and 41 being canceled by way of the present amendment. Under 35 U.S.C. §103, claims 28-31, 40 and 41 stand rejected over US 4,832,789 (Cochran et al), claims 32-34, 36 and 37 stand rejected over Cochran et al in view of US 5,612,254 (Mu et al), claim 35 stands rejected over Cochran et al in view of US 5,272,117 (Roth et al), and claims 38 and 39 stand rejected over Cochran et al in view of Roth et al and Mu et al. Claim 41 also was rejected under 35 U.S.C. §112, first paragraph.

The language of claim 421 incorporated into claim 40 has been amended to correct a typographical error leading to the §112 rejection.

The applicants greatly appreciate the courtesy of an interview granted to Applicants' representative by Examiner Eaton. First, Examiner Eaton explained that he was withdrawing the rejections over US Cochran et al. During the interview it was agreed that the combination of claims 28 and 29 and of 40 and 41 as set forth above would distinguish over the prior art of record, including the newly cited Chow, et al. (U.S. 4,789,648) patent. Examiner Eaton stated